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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/761,845	01/21/2004	G. Glenn Henry	CNTR.1356-CP1	3054

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HUFFMAN LAW GROUP, P.C.
1832 N. CASCADE AVE.
COLORADO SPRINGS, CO 80907-7449

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 03/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/761,845	HENRY ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The scope of meaning of claim 1 is not clear because it ends in a semicolon ";". Therefore also the scope of meaning of the claims that depend on claim 1 are also unclear.

Claim Rejections - 35 USC § 103

3. Claims 1-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Knebel (patent No. 6,618,801)in view of Blomgren (patent No. 5,695,009).

4. Knebel taught the invention substantially as claimed including a data processing ("DP") system comprising (As per claims 1,7,8,18):

a) Apparatus in a microprocessor for executing native instructions (e.g. see figs. 1-3 and col. 1, lines 34-61) ;

b) Instruction translation logic (fetch engine 20)(e.g., see figs. 1,2,3 and col. 1, lines 34-61) configured to retrieve macro instructions provided, and configured to translate each of the macro instruction into associated native instructions for execution wherein if a first form of the instruction is retrieved, the instruction translation logic (20)

directs the microprocessor to enable native bypass mode and indicates such by asserting a first bit (predecode bits)(e.g., see figs. 1,2,3) and col. 46-64);

c) Bypass logic (60,70) coupled to the instruction translation logic (20), configured to access a control bit (pre-decode bits) to determine if the native bypass mode is been enabled and to detect wrapper macro instructions and, upon detection of the wrapper macro instruction to provide the native instructions for execution by the microprocessor, thereby bypassing the instruction translation logic.(e.g., see fig. 2 and col. 1, lines 36-61 and col. 2, lines 29-56)[the fetch engine decodes the instruction that are macro instructions into microinstructions and directs emulation engine to bundle instructions and fetch engine separately sends instructions that are already microinstructions when fetched to multiplexer (70)[the logic within fetch unit that determined whether the instruction is a macroinstruction that would need decoding or already a microinstruction when fetch transmits the instruction that were already microinstructions and the one decoded via separate conductors one to the emulation engine and the other directly to the multiplexer provides for the claimed bypass operation[].

5. Knebel did not expressly detail that the translation logic was disabled. However one of ordinary skill would have been motivated to send each incoming instruction code via two parallel pipelines one for macroinstructions and one for instructions that were already microinstructions to take advantage of the possibility of the instruction already being a microinstruction that only needed to be forwarded increasing speed of production microinstructions. In order to do this when the instruction was a

microinstruction it would have been input to the macroinstruction decoder within the fetch unit. At that time one of ordinary skill would have been motivated to disable the decoder for translating the instruction and producing output because the decoding would produce an incorrect result and/or be redundant. All instructions whether instructions or microinstructions were in the same pipeline then the instructions that were already microinstruction would have to unnecessarily wait. Even if this type of system were employed when a microinstruction was input to the decoder an incorrect result would be produced and unnecessary delay would have been encountered. to disable the instruction translation logic,

6. Knebel did not expressly detail (1,8,11,14,19,22) asserting a first bit within a control register. Knebel did specify predecode bits (e.g., see col. 1, lines 36-61). However Blomgren taught when an instruction is not supported in the CISC instruction set signaling an exception and asserting a bit in a flags register to change to another mode for changing from instruction set types one of which was high level CISC and the other comprised microinstructions RISC (e.g., see col. 8,line 53-col. 9, line 29 and col. 10, lines 18-39). In this situation the emulation of CISC instructions using RISC instruction would have provided the microinstructions to the fetch unit in Knebel that would have by passed the decoder in the fetch unit (that translates macroinstructions). When the system finished executing the not supported instruction one of ordinary skill would have been motivated to reset the control bit for returning to CISC processing to process the remaining instructions within the program. Also since Blomgren taught setting flags bit for changing to a mode one of ordinary skill would have been motivated

to check the register to determine (FLAGS register) to determine the mode the system is in.

7. As to claims 12,13 Since Blomgren switched modes when an unsupported instruction was encountered then one of ordinary skill would have been motivated to return to the CISC mode when a supported instruction was encountered. That way if routine comprising plurality of instructions as to consecutively be translated the system would not unnecessarily change modes back and forth.

8. As to the receiving of instructions from an external bus It would have been obvious to one of ordinary skill that that the microprocessor of Knebel and Blomgren would have accessed instructions and data from external data from memory directly via a bus as was well known the art at the time of the claimed invention.

9. As to the embedding of the native instructions (claim 2,9) within wrapper, Sending of RISC instructions to the for execution and taught by Blomgren meets this limitation to the extent claimed. In addition Blomgren and Knebel taught a processor that can execute RISC and CISC programs. Knebel taught combining CISC and RISC registers. (e.g.,. see col. 15, line 13-col. 57). Therefore inorder to take advantage of availability of CISC instruction registers one of ordinary skill would have been motivated to format the RISC instructions for storage in the CISC registers. This would have provided an embedded instruction (e.g., see col. 15, lines 27-col. 16, line col. 17, lines 67).

10. As per claim 3,15 Knebel taught another bit (IF) within flags register to indicate the occurrence of an interrupting event (e.g., see col. 18,lines 18-39 and col. 6, lines 16-66).

11. As per claim 4,16 Knebel taught interrupt/exception/switch logic configured to clear the first bit within the control register upon occurrence of an interrupting even and prior to transferring control to an interrupt event service routine, thereby disabling the native bypass mode, and configured to assert the second bit (IF) within the flags register, thereby indicating occurrence of an interrupting event(e.g., see col. 10, lines 3-39).

12. As per claim 5,17,23 Blomgren taught (e.g. see col. 9, lines 21-29) an x86 EFLAGS register and that bits in the EFLAGS register that correspond to the CISC EFLAGS register is that are used during emulation of RISC instructions or other Native RISC instructions and are cleared at the end of when RISC emulation mode so the CISC instructions can access the EFLAGS register. The claimed bit 31 is within the reserved area of the EFLAGS register. Therefore one of ordinary skill would have been motivated to use the reserved area of the EFLAGS register to store the status bits to indicate the system is using the directly executed microinstruction (without needing translation) in the combined system.

13. As to claim 6,8 Knebel taught a fetch unit that detected to instruction type being fetched and provided for setting the processor to a mode for either decoding a macroinstruction or receiving a microinstruction and send the microinstruction to the instruction multiplexer bypassing the microinstruction translation (e.g., figs.1,2,3 and col.

see fig. 2 and col. 1, lines 36-61 and col. 2, lines 29-56) As to the embedding of the native instructions within wrapper, Sending of RISC instructions to the for execution and taught by Blomgren meets this limitation to the extent claimed. In addition Blomgren and Knebel taught a processor that can execute RISC and CISC programs. Knebel taught combining CISC and RISC registers. (e.g.,. see col. 15, line 13-col. 57). Therefore in order to take advantage of availability of CISC instruction registers one of ordinary skill would have been motivated to format the RISC instructions for storage in the CISC registers. This would have provided an embedded instruction (e.g., see col. 15, lines 27-col. 16, line col. 17, lines 67).

14. As to the further limitations of claims 10,20,21 the use of a loading instructions was well known in the art for loading data (which may comprise an effective address especially using indirect addressing). Therefore also since Blomgren taught processing x86 instructions then clearly it would have been obvious to one of ordinary skill that the CISC/RISC processing would have been used on any x86 instruction including load effective address. This is especially because Knebel taught that the use of encoding of the instructions as microinstructions would allow the system to more efficiently handle the processing of a series of instructions where if the buffer was not full the fetch unit send instructions directly to execution unit (e.g., col. 2, lines 8-28)[in this implementation clearly each instruction that was sent from the fetch unit would have corresponded to a valid macroinstruction. As to the placing of the microinstruction in the displacement field, since the macroinstruction would have comprised an opcode and operand when placing the microinstructions in the macroinstruction that was to be decoded one of ordinary

skill would have recognized that the opcode would have indicated to the system how to process the operand field. Therefore one of ordinary skill would have been motivated to place the microinstructions in the operand field. Depending on the type of instruction the operands would have comprised a data or address or displacement. One of ordinary skill would have been motivated to provide all instructions in a format that the decoder within the fetch unit could decode and that would have been with the microinstruction embedded in a CISC instruction.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Getzkaff (patent No. 5,898867) disclosed a DP system for correcting microcode (e.g. see abstract).

Huang (patent No. 6,243,786) disclosed a system for generating an interrupt prohibited zone in pipelined data processors (e.g. see abstract).

Wooten (patent No. 5,832,299) disclosed a system for emulating input/output devices utilizing processor with virtual system mode (e.g. see abstract).

Safford (patent No. 6,643,800) disclosed a DP system for testing microarchitecture features written by using tests written in microcode (e.g., see abstract).

Petsinger (patent No. 6,625,759) disclosed a system for verifying the fine-grained correctness of a behavioral mode (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EC

ERIC COLEMAN
PRIMARY EXAMINER